CLAIMS

WHAT IS CLAIMED:

1. An integrated semiconductor structure for testing a dielectric, said integrated semiconductor structure comprising:

a plurality of circuit elements, each having a first conductive region and a second conductive region separated by a dielectric to be tested;

a first contact pad electrically connected to said first conductive region, said first contact pad configured to be connected to an external instrument; and

a second contact pad electrically connected to said second conductive region, said second contact pad configured to be connected to said external instrument.

2. The integrated semiconductor structure of claim 1, wherein each of said second conductive regions is formed in a crystalline semiconductor region.

3. The integrated semiconductor structure of claim 2, wherein said crystalline semiconductor region further comprises a first and a second highly doped region that are separated by a lightly, inversely doped region.

4. The integrated semiconductor structure of claim 3, wherein said second contact pad is connected to said first and second highly doped regions.

5. The integrated semiconductor structure of claim 4, wherein said plurality of circuit elements each comprise at least one of a MOS transistor, a capacitor and a memory cell.

6. An integrated semiconductor structure for testing a dielectric, said integrated semiconductor structure comprising:

at least two circuit elements, each having a first electrode, a second electrode, a third electrode and a dielectric layer disposed adjacent to said first, second and third electrodes;

a first contact pad electrically connected to said first and second electrodes of said at least two circuit elements;

a second contact pad electrically connected to said third electrodes of said at least two circuit elements; and

a third contact pad electrically connected to a semiconductive region in which said circuit elements are at least partially formed.

7. The integrated semiconductor structure of claim 6, wherein at least some of said at least two circuit elements are substantially identical.

8. The integrated semiconductor structure of claim 6, wherein at least one of said at least two circuit elements differs from another one by at least one of size, type of circuit element, dopant profile and characteristics of the dielectric layer.

9. An integrated semiconductor structure for testing a dielectric, said integrated semiconductor structure comprising:

an N-channel transistor structure comprised of a gate electrode, a drain region and a source region;

a P-channel transistor structure comprised of a gate electrode, a drain region and a source region;

a first contact pad connected to said gate electrodes and said drain and source regions of said P-channel and N-channel transistor structures;

a second contact pad connected to a P-well of said N-channel transistor structure; and

a third contact pad connected to an N-well of said P-channel transistor structure.

10. The integrated semiconductor structure of claim 9, further comprising a plurality of N-channel transistor structures formed in said P-well.

11. The integrated semiconductor structure of claim 9, further comprising a plurality of P-channel transistor structures formed in said N-well.

12. A method, comprising:

commonly connecting first conductive regions of a plurality of circuit elements of a semiconductor structure with a first electric potential via a first common contact pad;

commonly connecting second conductive regions of said plurality of circuit elements of said semiconductor structure with a second electric potential via a second common contact pad, said first and second conductive regions being insulated from each other by a dielectric; and

assessing a reliability of said dielectric by determining failure events of said circuit elements.

13. The method of claim 12, wherein determining said failure events includes detecting abrupt changes of a signal indicative of a dielectric breakdown of said dielectric.

14. The method of claim 13, wherein said signal represents a leakage current through said dielectric.

15. A method, comprising:

commonly connecting source and drain regions of a plurality of transistor elements to a first electric potential by a first contact pad;

commonly connecting gate electrodes of said plurality of transistor elements to a second electric potential by a second contact pad;

connecting a common well region of said plurality of transistor elements to a third electric potential by a third contact pad; and

assessing a reliability of gate insulation layers of said plurality of transistor elements by monitoring a gate leakage current of said plurality of transistor elements.

16. A method, comprising:

commonly connecting source and drain regions and a gate electrode of at least one N-channel transistor structure and at least one P-channel transistor structure to a first electric potential by a first contact pad;

connecting a P-well region of said at least one N-channel transistor structure to a second electric potential by a second contact pad;

connecting an N-well region of said at least one P-channel transistor structure to a third electric potential by a third contact pad; and

assessing a reliability of gate insulation layers of said at least one N-channel transistor structure and said at least one P-channel transistor structure by determining a failure event.

17. The method of claim 16, wherein said second and third potentials are of opposite polarities.

18. The method of claim 17, wherein said second and third potentials are applied substantially simultaneously.

19. The method of claim 17, wherein said second and third potentials are applied sequentially.

20. The method of claim 19, wherein said second and third potentials are applied as pulses in an alternating manner.

21. The method of claim 16, wherein said failure event is determined by detecting abrupt changes of a signal indicative of a dielectric breakdown of a gate insulation layer of said at least one N-channel transistor structure and said at least one P-channel transistor structure.

22. The method of claim 21, wherein said signal represents a leakage current through said gate insulation layers.

23. A semiconductor test structure, comprising:

a plurality of test circuit elements each including a dielectric layer to be tested; and

a plurality of contact pads configured to connect an external measurement instrument to said plurality of test circuit elements;

wherein a design of interconnects providing electrical connection between said contact pads and said test circuit elements provides a ratio of the number of test circuit elements to the number of contact pads that is higher than 1:3.